

## IN THE CLAIMS:

Amend the claims as indicated below.

- 1 1. (original) A content addressable memory (CAM) device comprising:  
2 a first plurality of storage circuits to store an upper value;  
3 a second plurality of storage circuits to store a lower value; and  
4 a plurality of compare circuits to determine if a first comparand value is within a range  
5 of values defined by the upper value and the lower value.
- 1 2. (original) The CAM device of claim 1 wherein the first comparand value is a field of  
2 bits within a second comparand value.
- 1 3. (original) The CAM device of claim 1 wherein each of the first plurality of storage  
2 circuits includes a memory element to store at least one bit of the upper value.
- A<sub>2</sub>  
1 4. (original) The CAM device of claim 1 wherein each of the plurality of compare circuits  
2 includes circuitry to compare a bit of the first comparand to a bit of the upper value and  
3 to output a result signal in a first state if the bit of the first comparand is greater than the  
4 bit of the upper value and to output the result signal in a second state if the bit of the first  
5 comparand is less than the bit of the upper value.
- 1 5. (original) The CAM device of claim 4 wherein outputting the result signal in a first  
2 state comprises switchably coupling a match signal line to a predetermined voltage  
3 reference to affect a voltage level of the match signal line.
- 1 6. (original) The CAM device of claim 5 wherein outputting the result signal in the second  
2 state comprises decoupling the match signal line from the predetermined voltage  
3 reference.
- 1 7. (original) The CAM device of claim 5 wherein coupling the match signal line to a  
2 predetermined voltage reference comprises coupling the match signal line to a ground

3 voltage reference to pull down the voltage level of the match signal line.

1 8. (original) The CAM device of claim 4 further comprising a match line, and wherein a  
2 most significant compare circuit of the plurality of compare circuits is coupled to the  
3 match line, the most significant compare circuit being adapted to affect a logical state of  
4 the match line according to the result signal.

1 9. (original) The CAM device of claim 8 wherein the most significant compare circuit is  
2 coupled to output the result signal to the match line.

1 10. (original) The CAM device of claim 8 wherein at least one other of the plurality of  
2 compare circuits is coupled to output the result signal to the most significant compare  
3 circuit.

A<sub>2</sub>  
1 11. (original) The CAM device of claim 1 wherein the upper value comprises a plurality of  
2 bits ordered from a most significant bit to a least significant bit, and wherein each of the  
3 plurality of compare circuits is adapted to store a respective one of the plurality of bits  
4 and to compare the one of the plurality of bits to a respective bit within the first  
5 comparand value.

1 12. (original) The CAM device of claim 11 further comprising a match line and wherein a  
2 most significant compare circuit of the plurality of compare circuits is coupled to the  
3 match line, the most significant compare circuit including circuitry to affect a logical  
4 state of the match line if either (1) a most significant bit of the first comparand value is  
5 greater than the most significant bit of the upper value, or (2) the most significant bit of  
6 the first comparand is equal to the most significant bit of the upper value, and a result  
7 signal from a less significant compare circuit of the plurality of compare circuits  
8 indicates that the first comparand value minus the value represented by the most  
9 significant bit of the first comparand value is greater than the upper value minus the  
10 value represented by the most significant bit of the upper value.

1 13. (original) The CAM device of claim 1 wherein the lower value comprises a plurality of  
2 bits ordered from a most significant bit to a least significant bit, and wherein each of the  
3 plurality of compare circuits is adapted to store a respective one of the plurality of bits  
4 and to compare the one of the plurality of bits to a respective bit within the first  
5 comparand value.

1 14. (original) The CAM device of claim 13 further comprising a match line and wherein a  
2 most significant compare circuit of the plurality of compare circuits is coupled to the  
3 match line, the most significant compare circuit including circuitry to affect a logical  
4 state of the match line if either (1) a most significant bit of the first comparand value is  
5 less than the most significant bit of the lower value, or (2) the most significant bit of the  
6 first comparand is equal to the most significant bit of the lower value, and a result signal  
7 from a less significant compare circuit of the plurality of compare circuits indicates that  
8 the first comparand value minus the value represented by the most significant bit of the  
9 first comparand value is less than the lower value minus the value represented by the  
10 most significant bit of the lower value.

1 15. (currently amended) A content addressable memory (CAM) cell comprising:  
2 a first storage circuit to store a first boundary value; ~~and~~  
3 a first compare circuit to compare a comparand value to a the first boundary value, the  
4 first compare circuit including circuitry to output a first result signal in a first state  
5 if the comparand value is greater than the first boundary value and in a second  
6 state if the comparand value is less than the first boundary value; and  
7 an input to receive a second result signal from another CAM cell, and wherein the  
8 circuitry to output the first result signal in the first state is adapted to output the  
9 first result signal in the first state if the comparand value is equal to the first  
10 boundary value and the second result signal is in the first state.

1 16. (canceled)

- 1 17. (currently amended) The CAM cell of claim 15 ~~16~~ wherein the circuitry to output the  
2 first result signal is further adapted to output the first result signal in the second state if  
3 the comparand value is equal to the first boundary value and the second result signal is  
4 in the second state.
- 1 18. (original) The CAM cell of claim 15 further comprising:  
2 a second storage circuit to store a second boundary value; and  
3 a second compare circuit to compare the comparand value to the second boundary value,  
4 the second compare circuit including circuitry to output a second result signal in  
5 the first state if the comparand is less than the second boundary value and in the  
6 second state if the comparand is greater than the second boundary value.
- A<sub>2</sub>  
1 19. (original) The CAM cell of claim 18 further comprising an input to receive a third result  
2 signal from a less significant CAM cell, and wherein the circuitry to output the second  
3 result signal in the first state is further adapted to output the second result signal in the  
4 first state if the comparand value is equal to the second boundary value and the third  
5 result signal is in the first state.
- 1 20. (original) The CAM cell of claim 15 wherein the circuitry to output the first result  
2 signal is adapted to output the first result signal in the first state if the comparand is  
3 equal to the first boundary value.
- 1 21. (original) The CAM cell of claim 15 wherein the circuitry to output the first result  
2 signal is adapted to output the first result signal in the second state if the comparand is  
3 equal to the first boundary value.
- 1 22. (original) The CAM cell of claim 15 wherein the first boundary value is an upper  
2 boundary value.
- 1 23. (original) A content addressable memory (CAM) device comprising:

2 a first storage circuit to store a first value; and  
3 a compare circuit coupled to the first storage circuit to receive the first value and  
4 coupled to a mode signal line to receive a mode signal, the compare circuit being  
5 adapted to compare a comparand value to the first value and to output a first result  
6 signal, the first result signal indicating whether the comparand value is greater  
7 than the first value when the mode signal is in a first state, and the first result  
8 signal indicating whether the comparand is equal to the first value when the mode  
9 signal is in a second state.

A<sub>2</sub>  
1 24. (original) The CAM device of claim 23 further comprising a second storage circuit to  
2 store a second value and coupled to provide the second value to the compare circuit, the  
3 compare circuit including circuitry to compare the comparand value to the second value  
4 and to output a second result signal, the second result signal indicating whether the  
5 comparand is less than the second value when the mode signal is in the first state.

1 25. (original) The CAM device of claim 23 further comprising:  
2 a second storage circuit to store a second value and coupled to provide the second value  
3 to the compare circuit, the compare circuit including circuitry to compare the  
4 comparand value to the second value and, when the mode signal is in the first  
5 state, to output a second result signal indicating whether the comparand is less than  
6 the second value; and  
7 a mask circuit coupled to receive the second value from the storage circuit and coupled  
8 to the compare circuit, the mask circuit being adapted to selectively mask the first  
9 result signal, according to the second value, when the mode signal is in the second  
10 state.

1 26. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the  
2 first result signal by preventing the compare circuit from outputting the first result signal  
3 in a state indicative of inequality between the first value and the comparand.

1 27. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the

2 first result signal by disabling the first value from being received in the compare circuit.

1 28. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the  
2 first result signal by disabling the comparand value from being received in the compare  
3 circuit.

1 29. (original) A content addressable memory (CAM) device comprising:  
2 a first storage circuit to store a first value; and  
3 a first compare circuit coupled to receive the first value from the first storage circuit and  
4 having a select input to receive a level select signal, the first compare circuit being  
5 adapted to compare a comparand value to the first value and to assert a beyond-  
6 boundary signal if the level select signal is in a first state and if the comparand  
7 value is greater than the first value, the first compare circuit being further adapted  
8 to assert the beyond-boundary signal if the level select signal is in a second state  
9 and if the comparand value is less than the first value.

1 30. (currently amended) The CAM device of claim 29 further comprising:  
2 a ~~an~~ first input to receive a first signal representative of the comparand value;  
3 a second input to receive a second signal representative of a complement of the  
4 comparand value; and  
5 a select circuit coupled to the first input and the second input to select, according to a  
6 state of the level select signal, either the first signal or the second signal to be  
7 output to the compare circuit for comparison with the first value.

1 31. (original) The CAM device of claim 30 wherein the select circuit is a multiplexer  
2 having a control input coupled to receive the level select signal and having first and  
3 second ports coupled respectively to the first and second inputs.

1 32. (original) The CAM device of claim 29 wherein the first value is representative of an  
2 upper boundary value when the level select signal is in the first state, and wherein the  
3 first value is representative of a lower boundary value when the level select signal is in

4 the second state

1 33. (original) The CAM device of claim 29 further comprising a mode select input to  
2 receive a mode select signal, the first compare circuit being enabled to assert the  
3 beyond-boundary signal if the mode select signal is in a first state and the first compare  
4 circuit being disabled from asserting the beyond-boundary signal if the mode select  
5 signal is in a second state.

A 2  
1 34. (original) The CAM device of claim 33 further comprising a second compare circuit to  
2 compare the comparand value and the first value and to assert a match signal indicative  
3 of whether the comparand value is equal to the first value, the second compare circuit  
4 being enabled to assert the match signal if the mode select signal is in the second state,  
5 and the second compare circuit being disabled from asserting the match signal if the  
6 mode select signal is in the first state.

1 35. (original) A content addressable memory (CAM) device comprising:  
2 a CAM array having a plurality of CAM cells; and  
3 at least one mode select line coupled to at least one set of CAM cells within the plurality  
4 of CAM cells, the set of CAM cells being adapted to compare a comparand value  
5 to a range defined by at least one boundary value stored within the set of CAM  
6 cells if a mode select signal on the mode select line is in a first state, and the set of  
7 CAM cells being adapted to compare the comparand value for equality with a data  
8 value stored within the set of CAM cells if the mode select signal is in a second  
9 state.

1 36. (original) The CAM device of claim 35 further comprising a mode configuration circuit  
2 coupled to the mode select line, the mode configuration circuit including a storage  
3 circuit to store a mode value, the mode select signal being in either the first state or the  
4 second state according to the mode value.

1 37. (original) The CAM device of claim 36 further comprising an interface to receive a first

2 instruction from a host processor, the CAM device being adapted to store the mode  
3 value in the storage circuit in response to the first instruction.

1 38. (original) The CAM device of claim 36 further comprising a mode select interface, and  
2 wherein the mode select line is coupled to the mode select interface to receive the mode  
3 select signal from an external device.

1 39. (original) The CAM device of claim 38 wherein the external device is a host processor.

A<sub>2</sub>  
1 40. (original) A system comprising:  
2 a processor; and  
3 a content addressable memory (CAM) device coupled to receive instructions and data  
4 values from the processor, the CAM device including a plurality of CAM cells and  
5 being responsive to a first instruction from the processor to select either a first  
6 operating mode or a second operating mode for the plurality of CAM cells, the  
7 plurality of CAM cells being adapted to compare a comparand value to a range  
8 defined by at least one boundary value stored within the plurality of CAM cells if  
9 the first operating mode is selected, and the plurality of CAM cells being adapted  
10 to compare the comparand value for equality with a data value stored within the  
11 plurality of CAM cells if the second operating mode is selected.

1 41. (original) The system of claim 40 wherein the CAM device includes a mode  
2 configuration circuit to store a mode select value in response to the first instruction, the  
3 mode select value indicating the first operating mode or the second operating mode  
4 according to the first instruction.

1 42. (original) The system of claim 41 wherein the plurality of CAM cells is responsive to  
2 the mode select value to operate in either the first operating mode or the second  
3 operating mode.

1 43. (currently amended) The system of claim 41 wherein the CAM device includes



2 additional CAM cells configured to operate only in the first ~~second~~ operating mode.

1 44. (original) The system of claim 41 wherein the CAM device includes additional CAM  
2 cells configured to operate only in the second operating mode.

1 45. (original) A system comprising:  
2 a processor; and  
3 a content addressable memory (CAM) device coupled to receive instructions from the  
4 processor, the CAM device including a first plurality of CAM cells and being  
5 responsive to a first instruction from the processor to store a first boundary value  
6 in the first plurality of CAM cells, the first plurality of CAM cells being adapted to  
7 compare the first boundary value with a first comparand value in a compare  
8 operation and to output a first result signal indicative of whether the first  
9 comparand value is greater than the first boundary value.

1 46. (original) The system of claim 45 wherein the first plurality of CAM cells are  
2 responsive to a mode select signal to operate in either a range mode or a ternary mode,  
3 the first plurality of CAM cells being adapted to output the first result signal when  
4 operated in the range mode.

1 47. (original) The system of claim 45 wherein the first plurality of CAM cells are  
2 responsive to a mode select signal to operate in either a range mode or a binary mode,  
3 the first plurality of CAM cells being adapted to output the first result signal when  
4 operated in the range mode.

1 48. (currently amended) The ~~The~~ system of claim 45 wherein the CAM device further  
2 includes a second plurality of CAM cells to store a data value, the second plurality of  
3 CAM cells being adapted to compare the data value with a second comparand value in a  
4 compare operation and to output a first result signal indicative of whether the second  
5 comparand value is equal to the data value.

1 49. (original) The system of claim 48 wherein the first plurality of CAM cells and the  
2 second plurality of CAM cells are each included within a first row of CAM cells within  
3 the CAM device.

1 50. (original) The system of claim 48 wherein the first comparand value and the second  
2 comparand value each constitute a respective field of bits within a third comparand  
3 value.

A<sub>2</sub>  
1 51. (original) The system of claim 45 wherein the CAM device is further responsive to the  
2 first instruction from the processor to store a second boundary value in the first plurality  
3 of CAM cells, and the first plurality of CAM cells being further adapted to compare the  
4 second boundary value with the second comparand in the compare operation and to  
5 output a second result signal indicative of whether the first comparand value is less than  
6 the second boundary value.

1 52. (currently amended) The system of claim 45 wherein the CAM device includes multiple  
2 independently searchable storage blocks each including a plurality of CAM cells therein,  
3 the first plurality of CAM ~~claim~~ cells being included within the plurality of CAM cells  
4 in one of the searchable storage blocks.

1 53. (original) The system of claim 52 wherein the CAM device further includes a block  
2 configuration circuit to store a block configuration value, and circuitry to configure at  
3 least one of the storage blocks to have a storage width and depth according to the block  
4 configuration value.

1 54. (original) The system of claim 53 wherein the CAM device is responsive to a second  
2 instruction from the processor to store the block configuration value in the block  
3 configuration circuit.

1 55. (original) The system of claim 53 wherein the block configuration circuit is adapted to

2 store a mode value, and wherein the first plurality of CAM cells are responsive to the  
3 mode value to operate in either a range mode or a ternary mode, the first plurality of  
4 CAM cells being adapted to output the first result signal when operated in the range  
5 mode.

1 56. (original) The system of claim 55 wherein the CAM device is responsive to a second  
2 instruction from the processor to store the mode value in the block configuration circuit.

1 57. (original) The system of claim 53 wherein the block configuration circuit is adapted to  
2 store a mode value, and wherein the first plurality of CAM cells are responsive to the  
3 mode value to operate in either a range mode or a binary mode, the first plurality of  
4 CAM cells being adapted to output the first result signal when operated in the range  
5 mode.

A<sub>2</sub>  
1 58. (original) A method of operation within a content addressable memory (CAM) device,  
2 the method comprising:  
3 comparing a comparand value with a first boundary value stored in a plurality of CAM  
4 cells within the CAM device; and  
5 asserting a first result signal if the comparand value is greater than the first boundary  
6 value.

1 59. (original) The method of claim 58 further comprising storing the first boundary value in  
2 the plurality of CAM cells in response to a write instruction.

1 60. (original) The method of claim 58 wherein comparing the comparand value with the  
2 first boundary value comprises, in each CAM cell of the plurality of CAM cells,  
3 asserting a greater-than signal if either (1) a bit of the comparand value received within  
4 the CAM cell is greater than a bit of the first boundary value stored within the CAM  
5 cell, or (2) the bit of the comparand value is equal to the bit of the first boundary value  
6 and a greater-than signal is received from a less significant CAM cell within the  
7 plurality of CAM cells.

- A<sub>2</sub>
- 1 61. (currently amended) The method of claim ~~58~~ 61 wherein a greater-than signal asserted  
2 by a most significant one of the plurality of CAM cells constitutes the first result signal.
- 1 62. (original) The method of claim 58 further comprising:  
2 comparing a comparand value with a second boundary value stored in the plurality of  
3 CAM cells; and  
4 asserting a second result signal if the comparand value is less than the second boundary  
5 value.
- 1 63. (original) The method of claim 62 wherein comparing the comparand value with the  
2 second boundary value comprises, in each CAM cell of the plurality of CAM cells,  
3 asserting a less-than signal if either (1) a bit of the comparand value received within the  
4 CAM cell is less than a bit of the second boundary value stored within the CAM cell, or  
5 (2) the bit of the comparand value is equal to the bit of the second boundary value and a  
6 less-than signal is received from a less significant CAM cell within the plurality of  
7 CAM cells.
- 1 64. (original) The method of claim 63 wherein a less-than signal asserted by a most  
2 significant one of the plurality of CAM cells constitutes the second result signal.
- 1 65. (original) A content addressable memory (CAM) device comprising:  
2 means for comparing a comparand value with a first boundary value stored in a plurality  
3 of CAM cells within the CAM device; and  
4 means for asserting a first result signal if the comparand value is greater than the first  
5 boundary value.
- 1 66. (original) The CAM device of claim 65 further comprising means for storing the first  
2 boundary value in the plurality of CAM cells in response to a write instruction.
- 1 67. (original) The CAM device of claim 65 wherein the means for comparing a comparand

2 value with a first boundary value comprises respective means within each CAM cell of  
3 the plurality of CAM cells for asserting a greater-than signal if either (1) a bit of the  
4 comparand value received within the CAM cell is greater than a bit of the first boundary  
5 value stored within the CAM cell, or (2) the bit of the comparand value is equal to the  
6 bit of the first boundary value and a greater-than signal is received from a less  
7 significant CAM cell within the plurality of CAM cells.

A<sub>2</sub>  
1 68. (original) The CAM device of claim 65 further comprising:  
2 means for comparing a comparand value with a second boundary value stored in the  
3 plurality of CAM cells; and  
4 means for asserting a second result signal if the comparand value is less than the second  
5 boundary value.

1 69. (original) The CAM device of claim 68 wherein the means for comparing a comparand  
2 value with a second boundary value comprises respective means within each CAM cell  
3 of the plurality of CAM cells for asserting a less-than signal if either (1) a bit of the  
4 comparand value received within the CAM cell is less than a bit of the second boundary  
5 value stored within the CAM cell, or (2) the bit of the comparand value is equal to the  
6 bit of the second boundary value and a less-than signal is received from a less significant  
7 CAM cell within the plurality of CAM cells.

1 70. (new) A CAM device comprising:  
2 at least one range compare cell configured to store a bit of a range limit, wherein the at  
3 least one range compare cell is further configured to output a result signal that  
4 indicates at least whether the stored range limit bit is greater than or less than a  
5 corresponding bit of a comparand; and  
6 at least one CAM cell configured to store a data bit, wherein the at least one CAM cell is  
7 further configured to output a match signal that indicates whether the stored data  
8 bit matches a corresponding bit of a comparand, wherein at least one range  
9 compare cell and at least one CAM cell are coupled to a common match line.

1 71. (new) The CAM device of claim 70 wherein the at least one CAM cell comprises a  
2 ternary CAM cell.

1 72. (new) The CAM device of claim 70 wherein the at least one CAM cell comprises a  
2 binary CAM cell.

1 73. (new) The CAM device of claim 70 wherein the at least one range compare cell  
2 comprises a configurable cell that selectively operates in one of a range compare cell  
3 mode and a ternary CAM cell mode.

1 74. (new) The CAM device of claim 70 wherein the at least one range compare cell  
2 comprises a configurable cell that selectively operates in one of a range compare cell  
3 mode and a binary CAM cell mode.

1 75. (new) The CAM device of claim 70 wherein the at least one range compare cell  
2 comprises:  
3 at least one less significant range compare cell configured to output the result signal to a  
4 next more significant range compare cell, wherein the result signal is dependent on  
5 a result of a comparison of the stored range limit bit and the corresponding  
6 comparand bit, and a result signal output from a next less significant range  
7 compare cell; and  
8 a most significant range compare cell configured to output a final result signal to the  
9 common match line, wherein the final result signal indicates at least whether the  
10 comparand is greater than or less than the stored range limit.

1 76. (new) The CAM device of claim 70 wherein the result signal further indicates whether  
2 the stored range limit bit is equal to a corresponding comparand bit .

1 77. (new) The CAM device of claim 75 wherein the final result signal output to the  
2 common match line further indicates whether the stored range limit is equal to the

3 comparand.

1 78. (new) A method for performing a range comparison operation in a content addressable  
2 memory (CAM) device to determine whether a comparand is within a range, the method  
3 comprising:

4 storing at least one range limit in a plurality of range compare cells, including a most  
5 significant range compare cell, and a plurality of less significant range compare  
6 cells for storing bits of the range limit according to their significance;

7 comparing bits of the comparand with corresponding bits of the range limit;

8 outputting a result signal for each range compare cell based on the bit comparison, and  
9 on a result signal output by a next less significant range compare cell; and

10 outputting a final result signal from the most significant range compare cell to a match  
11 line, wherein the final result signal indicates at least whether the comparand is  
12 greater than or less than the range limit.

1 79. (new) The method of claim 78 wherein the at least one range limit includes an upper  
2 range limit, and wherein the final result signal indicates the comparand is within the  
3 range when the comparand is less than the upper range limit.

1 80. (new) The method of claim 78 wherein the at least one range limit includes a lower  
2 range limit, and wherein the final result signal indicates the comparand is within the  
3 range when the comparand is greater than the lower range limit.

1 81. (new) The method of claim 78 wherein the at least one range limit includes an upper  
2 range limit, and wherein the final result signal indicates the comparand is within the  
3 range when the comparand is less than the upper range limit or equal to the upper range  
4 limit.

1 82. (new) The method of claim 78 wherein the at least one range limit includes a lower  
2 range limit, and wherein the final result signal indicates the comparand is within the  
3 range when the comparand is greater than or equal to the lower range limit.

1 83. (new) The method of claim 78 wherein the at least one range limit includes a lower  
2 range limit and an upper range limit, and wherein the final result signal indicates the  
3 comparand is within the range when the comparand is greater than the lower range limit  
4 and less than the upper range limit.

1 84. (new) The method of claim 78 wherein the at least one range limit includes a lower  
2 range limit and an upper range limit, and wherein the final result signal indicates the  
3 comparand is within the range when the comparand is greater than or equal to the lower  
4 range limit and less than or equal to the upper range limit.

A<sub>2</sub>  
1 85. (new) The method of claim 78 wherein the plurality of range compare cells comprises a  
2 plurality of configurable cells, including a most significant configurable cell, and a  
3 plurality of less significant configurable cells for storing bits of at least one stored value  
4 according to their significance, the method further comprising, setting a mode select  
5 signal to select a range compare mode or a ternary CAM mode, wherein, in the ternary  
6 CAM mode, the at least one stored value comprises a data word and a mask word, and  
7 wherein, in the range compare mode, the at least one stored value comprises an upper  
8 range limit and a lower range limit;

1 86. (new) The method of claim 85, further comprising:  
2 in the ternary CAM mode,  
3 comparing a comparand bit with a masked data bit in each of the plurality of  
4 configurable cells; and  
5 outputting a result signal based on the comparison from each configurable cell to  
6 the common match line; and  
7 in the range compare mode,  
8 comparing a comparand bit with an upper range bit in each of the plurality of  
9 configurable cells;  
10 comparing a comparand bit with a lower range bit in each of the plurality of  
11 configurable cells;



A 2  
12 outputting a first result signal from each less significant configurable cell to a next  
13 more significant configurable cell based on the lower range comparison and on  
14 a first result signal from a next less significant configurable cell;  
15 outputting a second result signal from each less significant configurable cell to a  
16 next more significant configurable cell based on the upper range comparison  
17 and on a second result signal from the next less significant configurable cell;  
18 outputting a first final result signal from the most significant configurable cell to  
19 the common match line based on based on the lower range comparison and on  
20 a first result signal from a next less significant configurable cell; and  
21 outputting a second final result signal from the most significant configurable cell  
22 to the common match line based on the upper range comparison and on a  
23 second result signal from the next less significant configurable cell.

1 87. (new) A content addressable memory (CAM), comprising:  
2 a match line; and  
3 a plurality of CAM cells including storage circuits to store an upper bound value and a  
4 lower bound value and compare circuits coupled to the storage circuits, wherein  
5 the plurality of CAM cells are coupled in a chain ordered from a least significant  
6 compare circuit to a most significant compare circuit to compare a comparand  
7 value with the upper and lower boundary values, and to resolve a compare result  
8 from the least significant compare circuit to the most significant compare circuit,  
9 and wherein the most significant compare circuit couples the plurality of CAM  
10 cells to the match line.